VERILOGIC PRELIMS

Rules and Regulations **Marks: 45**

- Answer all questions
- The solutions should have neat diagrams with necessary brief explanations
- The marks of each question is specified in the brackets
- Mail the solutions to 108106025@nitt.edu (with subject as Verilogic)
- For doubts contact

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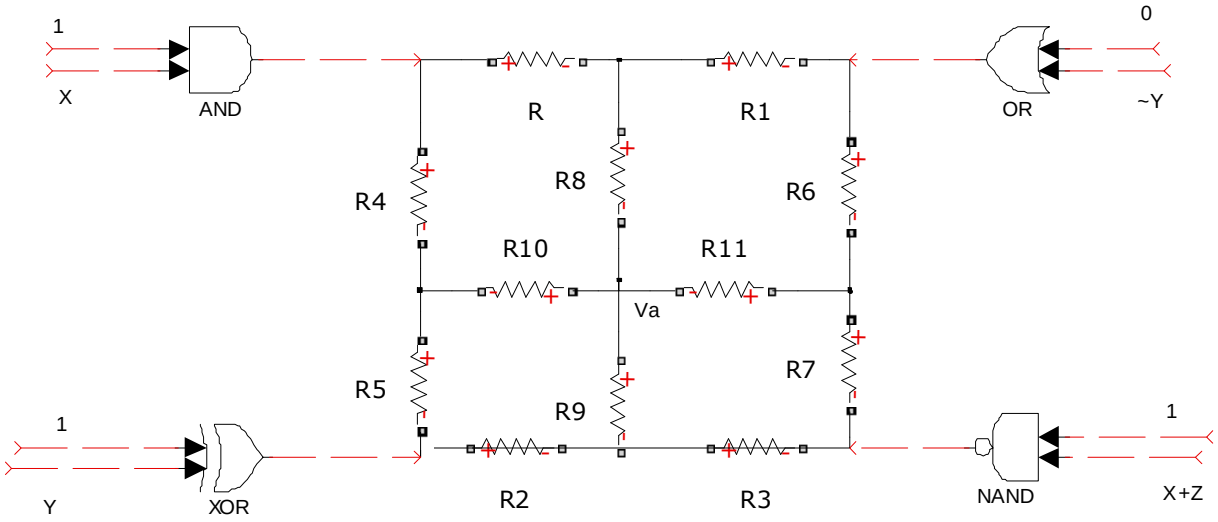
1. Implement Y=A.B+C.D, given that(2)
   I. A and B arrive at t=0
   II. C comes at t=1ns
   III. D comes at t=2ns
   IV. MUX, Adder and logic gates have 1ns propagation delay
   V. Output Y should be available at t=3ns

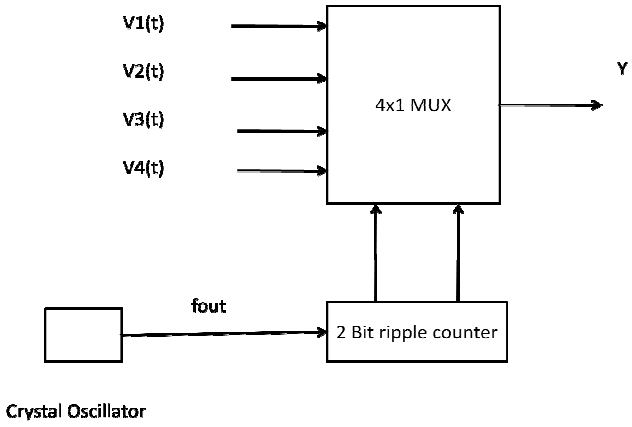
2. What is the number of unused inputs in a BCD adder for a single digit with carry?(2)

3. Give a combinational circuit that doubles the input clock frequency.(1)

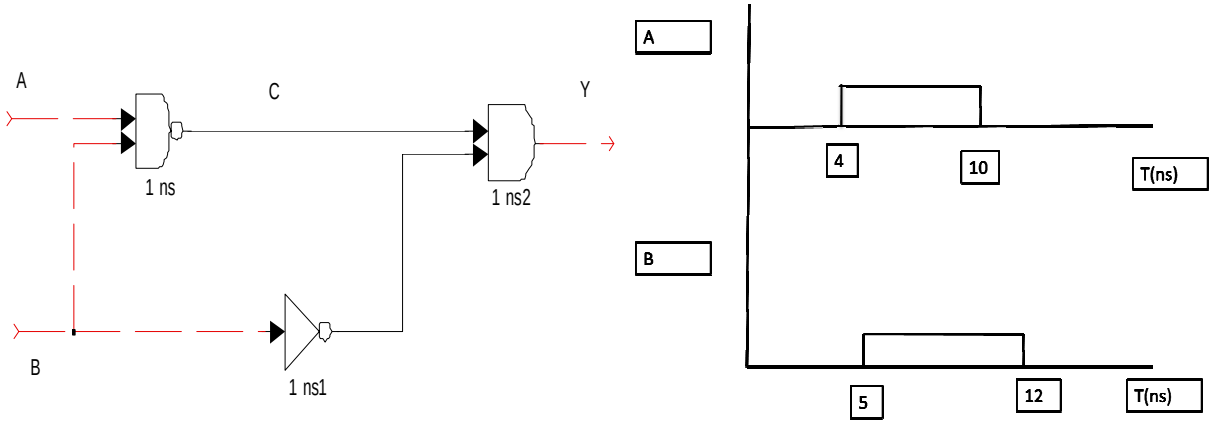
4. In the circuit, given that when the output of a gate is high, it is at 5V and at when it is low it is at 0V. Find the value of x,y,z so that Va=3.75V. (All resistance value are equal to R and Va is at the center of the network)(3)



5. What is the minimum frequency fout to get a demultiplexed output?(2)
   Given,
   V1(t)=10sin400πt
   V2(t)=+5v, 0<t≤5 ms
   -5v, 5≤t<10 ms
   V3(t)=5v DC
   V4(t)=40cos1400πt
   Give reasons for your answer

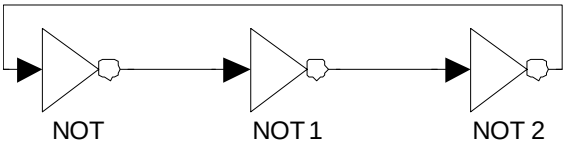


6. Give the timing diagram for Y and other intermediate lines (2)



7. The probability for A,B,C,D to be high is 0.5. What is the probability for F to be high F=AB+BC+A`CD?(1)

8. Three NOT gates are connected as shown in the figure. What will be the frequency of F if delay of each gate is 1 μs? What is the duty cycle of the wave at the output of each of the NOT gates?(2)



9. Which of the following logic families has the highest frequency of operation?(1)
   - I. ECL
   - II. TTL
   - III. CMOS
   - IV. I^2L
   - V. DTL

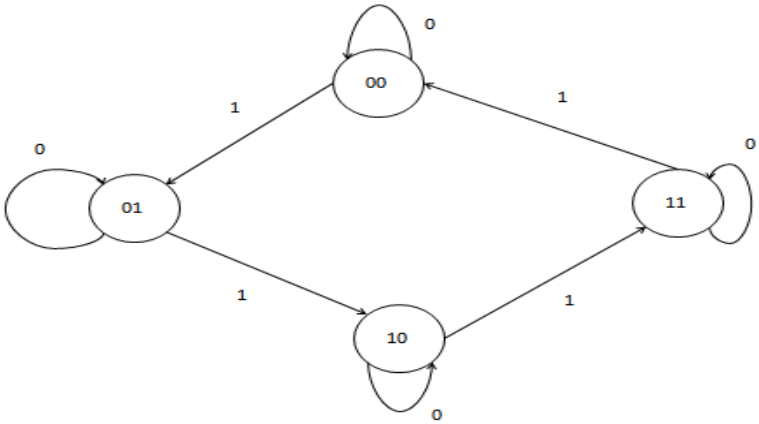
10. Draw the state diagram to generate 2's complement of a number considering the bits arrive serially(2)

11. Design a divide by 2 counter with 75% duty cycle.(2)

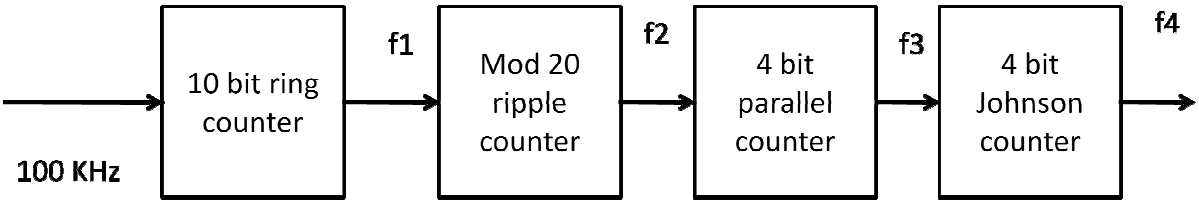
12. Design a combinational circuit using ROM that accepts a 3 bit number as input and produces an output that is the square of input. Mention the minimum size of ROM.(3)

13. You have three delay elements D1,D2,D3 that delay a clock by 25%, 50%, 75% respectively. Use only combinational circuit with delay elements to get twice the input frequency.(2)

14. For the following state diagram, draw state table, excitation table and design using JK flip-flop(3)



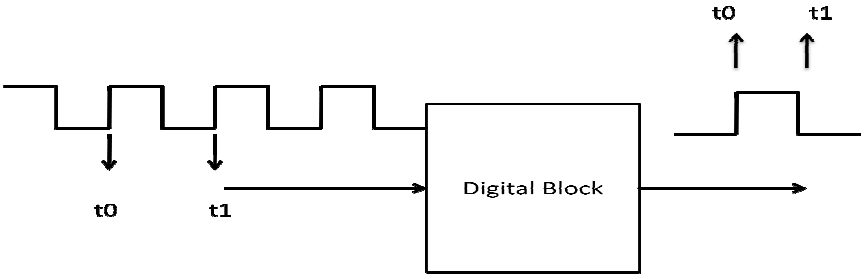
15. Find the output frequency f1=? f2=? f3=? f4=? (2)



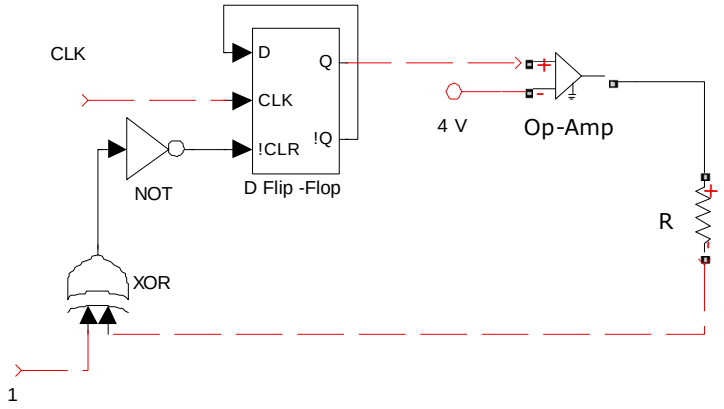
16. Realize JK flipflop with the following flipflop(2)

A	B	Q(n+1)
0	0	Q'(n)
0	1	1
1	0	0
1	1	Q(n)

17. Realize the following digital block (2)



18. Draw the waveform at point Q. Assume Q is initially zero and the supply voltage to opamp is 5V (2)



19. Draw the state diagram for the control circuit of a CD player. The player has the following switches – supply mains M, play P, stop S, song increment I, song decrement D and an alert bulb B. the CD player is active only if M is on. When mains M is on then on pressing P the present song can be played or by pressing I the song can be incremented etc. Pressing S stops the execution of the present task. When one operation is being done if you press the other switch the previous switch toggles automatically unless its toggling is prevented intensionally. At a given time if any two switches are intensionally tried to press simultaneously the bulb B should glow. (5)

20. Design a circuit which will detect palindrome of 4 bits.(1)

21. You are given a clock pulse of 300Hz and 50% duty cycle. Can you generate a waveform of 100 Hz frequency and 50% duty cycle using this clock with a sequential circuit.(3)